

Appl. No. 10/773,482
Amendment dated September 11, 2006
Reply to Office action of April 10, 2006

REMARKS/ARGUMENTS

Claims 1 through 20 were pending in this application.

The present Amendment amends independent claims 1 and 12.

Reconsideration and favorable action are respectfully requested.

Amendments to the Specification

Various typographical matters are corrected in the Specification, as summarized in the following table:

paragraph number	Correction(s)
0005	"resent" changed to "reset," consistent with numerous other uses of "reset" in the Specification (see, e.g., paragraphs 0007, 0034, 0042)
0030	"Figure 4" changed to "Figure 4A"
0049	Comma deleted in "parameter , and/or..."
0062	"he" replaced with "the"

Rejections Under 35 U.S.C. § 102(b)

Claims 1-9 and 11-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Hattori (US Patent 5,521,876; hereafter, "Hattori"). Claims 1 and 12 are amended only in form to include two commas, which is not considered in any way a limitation, narrowing, or change subject to disclaimer or prejudice but instead is made solely to facilitate the discussion provided below. And, given that discussion, Applicants respectfully request withdrawal of the present rejection of the claims.

Certain context is first provided for claim 1, and with that context a later discussion illustrates why claim 1 is not anticipated by Hattori. Claim 1 recites "a memory structure comprising a plurality of memory word addresses," and an example of such a structure is illustrated in Figures 2A through 2N. The Specification discusses this structure in detail. To support the terminology in claim 1, various aspects of the Specification are here summarized. Figures 2A through 2E illustrate the writing of words into what is referred to in both the Specification and claim as "word address" locations in the memory.¹ In the Specification, under non-overflow conditions, this writing is described as from the bottom of the memory structure upward, where each word address

¹ Specification, paragraph 0034, using the reference of WA[0] through WA[15] in Figures 2A through 2D.

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provides a word slot that is one word wide. Thus, "[e]ach immediately successive word is written into an immediately successive word address."² Thus, in the manner shown in these figures, each word is written into one respective horizontal word address. However, when an overflow occurs, as is detected in Figure 2F, "then the next word written to FIFO 12 is not written along a single word address, but instead that data is written across multiple word addresses."³ In other words, when the overflow occurs, then "it may be said that [the next] word ... is written vertically into FIFO 12, as compared to the horizontal nature of each individual word address."⁴ The preceding example is illustrated with the writing of word WD₂₂ in Figure 2F. Note that in the data sequence, word WD₂₂ follows word WD₂₁, where that preceding word WD₂₁ was written horizontally into the word address WA[5]. However, that next successive data word following word WD₂₁, namely word WD₂₂, is written vertically, and as shown in Figure 2F it therefore extends *across multiple word addresses* WA[6] through WA[13]. Indeed, this concept is further illustrated in Figures 2G through 2I, where each of word WD₂₂, word WD₂₃, and word WD₂₄ is also written in a manner that is described as vertically and that also may be characterized as written to extend *across multiple word addresses* WA[6] through WA[13]. Lastly, note that the preceding is supported in numerous other locations in the Specification, including in the discussion of the methods of operation (see, e.g., step 122 in Figure 3b and steps 502 versus 504 in Figure 5).

The distinctions noted above with respect to writing certain words in respective word addresses versus writing other words across multiple word addresses in borne out in claim 1. Particularly, claim 1 includes the following with respect to writes during a non-overflow condition:

control circuitry, operable during a non-overflow condition of the memory structure, for *writing successive ones* of received data words *into respective successive ones of the memory word addresses*;

In contrast, however, claim 1 further includes the following with respect to writes during an overflow condition:

control circuitry, operable during an overflow condition of the memory structure, for *writing each data word_i* in successive ones of received data words, *across multiple ones of the memory word addresses*.

In the present amendment, commas are added to this last subparagraph with the intent that the Examiner should fully understand this language. Particularly, it is clearly recited that "during an overflow," the recited circuitry is "for writing each data word ... across multiple ones of the memory word addresses." Again, with

² Specification, paragraph 0035.

³ Specification, paragraph 0039.

⁴ *Id.*

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reference to the Specification discussed above, an example of this last claim paragraph is readily seen when the data word WD₂₂ is written across the multiple memory word addresses WA[6] through WA[13].

Turning now to Hattori, the Examiner states that "The words will continue to be written across multiple memory word addresses (rows) when Y is incremented (Col 7, Lines 47-59))." The Examiner is correct that once a row is filled in Hattori, then the next write is to the next row, but this has nothing to do with writing one word across multiple word addresses. Indeed, Hattori explicitly states the following in describing its writing circuitry:

In operation, fixed-length data consisting of (m+1) words input from the host CPU one word at a time is input to the row pointed to by the Y pointer 34 in sequence starting at column address 0 as pointed to by the X pointer 32. When the column address pointed to by the X pointer 32 reaches m, the row address pointed to by the Y pointer is incremented by one.⁵

Thus, Hattori appears to write one word at a time into one column in a row. When a word is written into the last column of that row, the row pointer increments, and the next word is similarly written into one column of the next row. Thus, the Hattori embodiments cited by the Examiner do not write, as recited in claim 1, "each data word ... across multiple ones of the memory word addresses" during an overflow condition.

For the reasons described above, Applicant respectfully submits that amended claim 1 is not anticipated by Hattori and, thus, Applicant respectfully requests withdrawal of the rejection of amended claim 1 and its dependent claims 2 through 11.

Turning to method claim 12, it includes amended language comparable to that of amended claim 1. Accordingly, for reasons similar to claim 1 set forth above, Applicant respectfully submits that claim 12 is not anticipated by Hattori. Thus, Applicant respectfully requests withdrawal of the rejection of claim 12 and its dependent claims 13 through 20.

Fees

A Petition for a two month extension of time is submitted herewith, thereby extending the deadline to respond from July 10, 2006 to September 10, 2006, and with the latter date falling on a Sunday, thereby extending the deadline to September 11, 2006. The Commissioner is authorized to charge the fee for said Petition, and any other fees necessary to effect the present filing, to Deposit Account 20-0668 of Texas Instruments Incorporated.

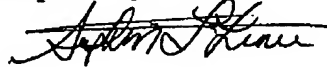
⁵ Hattori, col. 8, lines 13-19.

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Conclusion

Applicant respectfully requests that a timely Notice of Allowability be issued in this case.

Respectfully submitted,



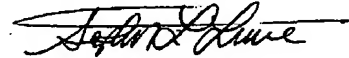
Stephen L. Levine
Registry No. 33,413

Anderson, Levine & Lintel, L.L.P.
14785 Preston Road, Suite 650
Dallas, Texas 75254
(972) 664-9552
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CERTIFICATE OF FACSIMILE TRANSMISSION
37 C.F.R. 1.8

The undersigned hereby certifies that this correspondence is being transmitted via facsimile, on September 11, 2006, to the United States Patent Office and more particularly to the Patent Office Central FAX Number of 571-273-8300 and addressed to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450



Stephen L. Levine
Registry No. 33,413